UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/931,125	09/16/1997	HAE-SEUNG LEE	P54508	3842

7590 11/04/2002

ROBERT E BUSHNELL
1522 K STREET, N.W. SUITE 300
WASHINGTON, DC 200051202

EXAMINER	
PORTKA, GARY J	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 36

Application Number: 08/931,125
Filing Date: September 16, 1997
Appellant(s): LEE, HAE-SEUNG

MAILED

NOV 04 2002

Technology Center 2100

Robert E. Bushnell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 28, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that Group I (claims 1-2 and 6), Group II (claims 7-8), and Group III (claims 3-5) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,572,660	JONES	11-1996
5,455,934	HOLLAND ET AL.	10-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. Claims 1-2 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones, U.S. Patent 5,572,660.

2. As to claim 1, Jones discloses *a RAID 5 memory system comprising*:

a. *Plurality of defect-adaptive devices* (214-1 through 214-8) as claimed *having a first region sequentially storing parity information needed for data recovery, and a second region storing data* (see Figure 2D, and column 10 lines 7-18);

b. *Plurality of caches* (254-1 through 254-8) *respectively coupled one-to-one to the devices, each for storing parity information blocks needed for data recovery for the corresponding device* (see Figure 2D, and column 10 lines 15-26);

c. *Controller* (210) *coupled to each device and cache, with means for selectively controlling writing, reading, and obtaining of parity information to/from each memory device, and storing parity information obtained from a device in a corresponding cache* (see Figure 3E, column 2 line 62 through column 4 line 6, in

particular column 3 lines 30-39; column 10 lines 15-26, and column 11 line 55 to column 12 line 13).

3. As to claim 2, Jones discloses that the controller *comprises means for determining if the information needed for data recovery is in the cache* (see Figure 3D item 344, and Figure 3E item 370).

4. As to claim 6, Jones discloses *a RAID 5 system comprising:*

a. *Plurality of disk drives* (214-1 through 214-8) *with a region storing data blocks and a region having a predetermined number of blocks for storing parity information* (see Figure 2D, and column 10 lines 7-18);

b. *Plurality of caches* (254-1 through 254-8) *each connected one-to-one to a corresponding drive and storing parity information* (see Figure 2D, and column 10 lines 15-26); c. *Controller* (210) *coupled to each disk drive and cache selectively controlling write of data and parity comprising means to*:

i. *Select a disk drive upon receiving write instruction (first means)* (see Figure 3A items 304, 308 and 330);

ii. *Read old data from the disk drive (second means)* (see Figure 3C item 360);

iii. *Determine if old parity to be read from disk is accessed in the corresponding cache (third means), and if not then to read the old parity from the disk drive, and load the cache with old parity (fourth means)* (see Figure 3E items 370, 376-382, and column 11 line 55 to column 12 line 13);

iv. *Obtain new parity by performing XOR on old data, old parity and new data (fifth means)* (see Figure 3F item 390, and column 9 line 16 equation);

v. *Load the corresponding cache with new parity (sixth means)* (see Figure 3F item 392);

vi. *Write the new data and new parity on the disk drive (seventh means)* (see Figure 3F item 394, and column 3 lines 25-40), *thus completing the writing* process.

5. As to claim 7, Jones discloses the *method for writing and reading a RAID 5 as recited, including sequentially storing information for data recovery in a first region of a disk, storing data in a second region, controlling writing, reading, and caching of information, the step for reducing overhead during read of data for recovery to improve data I/O performance* met by the functionally equivalent elements performing the steps described above with regard to claims 1-2 and 6. Appellant's own specification at page 6 lines 16-20 describes that two time reading and writing of disk drives is required when updating data with parity, which results in a large overhead. Jones also teaches a step for reducing overhead during a read for data recovery by avoiding the need to access the disk two times when the required data is in a cache, and by using the same structure and method as Appellant, as described above for example with regard to the entirety of claim 6.

6. As to claim 8, Jones discloses *coupling caches one-to-one to disks, and to the controller, storing data recovery information for each disk to its corresponding cache*, as described above with regard to claims 1-2 and 6. The *determining of information*

needed for recovery in a disk by using information for data recovery stored in the corresponding cache is described at Figure 3F item 390 and column 9 line 16 equation (in Figure 3D, a cache hit in the write back cache at 344 means that old parity is in the cache, which is read to perform the calculation at 390 of Figure 3F).

Claim Rejections - 35 USC § 103

7. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones, U.S. Patent 5,572,660, in view of Holland et al., U.S. Patent 5,455,934.

8. As to claim 3, Jones does not disclose that *the information needed for data recovery is sequentially arranged from the most outer cylinder.* However, it was notoriously well known in the art that disks are most efficiently accessed sequentially since this avoids or reduces seek time; it is further clear that a sequential access must start from some position on the disk. As taught by Holland, arrangement of information on a disk from the outermost cylinders results in higher sustained data transfer rates (see column 9 lines 25-30). Since, as taught by Jones at column 2 lines 34-58, the accessing of the parity data in RAID systems limits the performance of these systems, the advantage of faster access due to reduced seek time, and higher sustained data rates would have motivated an artisan to arrange this information from the outermost cylinder. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to sequentially arrange the recovery information from the most outer cylinder in Jones, because this method reduces seek time, and results in higher

sustained data rates for the data most limiting the performance, and therefore most efficiently improves the performance.

9. As to claim 4, Jones discloses that *parity information needed for data recovery is modified to a value obtained through a calculation of new data recovery information* (see column 9 lines 8-21).

10. As to claim 5, Jones discloses XORing of previous data, corresponding parity information, and new data (see column 9 line 16 equation).

(11) Response to Argument

Appellant argues that Jones does not teach that a unique one cache corresponds to a unique one disk, in a one-to-one caching for a RAID 5 system. The Examiner disagrees; the Abstract states that each drive has a "dedicated" cache, and the embodiment of Figure 2D is described as "similar to that of FIG. 2 with the exception that the parity information is stored and distributed among the plurality of disk drives...". Figure 2D clearly shows one cache for each disk. It is irrelevant, as argued, how the ellipsis of Figure 2D is to be interpreted; since the disks and caches shown are arranged in a one-to-one configuration, the claim language is met. Even so, the Examiner maintains that one of ordinary skill in the art would have taken the ellipsis to signify a continuation of the existing structure as shown, which is, throughout the entire disclosure, that each one cache is connected to a unique disk in a one-to-one connection as recited (see Figures 2 through 2D). It would be counter to this teaching

to assume that any cache is connected other than as shown in their one-to-one connection.

Appellant argues that claim 7 is a step-plus-function claim and as such, incorporates the structure described in the disclosure (or the equivalent thereof) as performing the function. As stated previously and herein, it appears that the structure that performs this function is intended to be as recited in the present claims. It is further noted as stated above that the present specification at page 6 lines 16-20 defines the large overhead as the two time reading and writing required on the prior art disk drives when updating data and parity. The Appellant's step for reducing overhead then must be the use of the caches to avoid the need to read and write the disk drives when possible, as described for example most comprehensively in claim 6. Since the structure of one-to-one caching as provided by claim 6 is rejected over Jones, it is therefore maintained that the function and equivalent structure that reduces overhead is also met by Jones.

Appellant argues that there is no specific teaching nor motivation in the prior art for combining Jones and Holland, and that proper evidence of sequential transfer for disks was not presented. The Examiner does not agree; the art of record establishes that the outer tracks of a disk offer improved performance, and as stated in previous actions it was well known that disks are most efficiently accessed sequentially. That is, it was well known that placing data randomly, irregularly, or otherwise non-sequentially on a disk would reduce performance; the rotation of a disk past a head, and the radial movement of the head to different tracks is inherently a sequential process. Thus it

would have been obvious to one of ordinary skill in the art to sequentially arrange, beginning at the outermost track, the performance-limiting data. It is well known in the art, and common sense, that performance-limiting data be configured or stored in such a manner as to be accessed faster than other data, in the same manner for example as data which is frequently or recently accessed gets stored into a cache. As cited, Jones teaches that the parity data is such performance-limiting data, and therefore the rationale for the combination (of accessing the parity data of Jones sequentially from the outer tracks) is maintained.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Gary J Portka

Gary J. Portka
Primary Examiner
AU 2188
11/1/02

CONFEREES

David Robertson
Primary Examiner
AU 2186

DoHyun Yoo
Do H. Yoo
Supervisory Patent Examiner
AU 2187

Robert E. Bushnell
1522 K Street N.W., Suite 300
Washington, DC 20005